16.1 A 4.5mW Closed-Loop ΔΣ Micro-Gravity CMOS-SOI Accelerometer

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Recently, there has been an increasing demand for low-power and small form-factor micro- and sub-micro-gravity accelerometers for a variety of applications including measurement of vibration, inertial navigation and geophysical sensing. High-performance micro-accelerometers can also be utilized in ultra-small size for large-volume portable applications such as laptop computers and cellular phones. A micro-g (*g*: *gravity*) accelerometer should maintain high performance, resolution and stability even in the presence of large accelerations such as earth gravity. In open-loop systems, the dynamic range is limited and the performance degraded when large background accelerations exist [1]. Therefore, closed-loop operation of the micro-accelerometer is essential to improve dynamic range and linearity.

In this work, the implementation and characterization of a force-rebalanced high-order ΔΣ micro-accelerometer with micro-gravity resolution and stability and an extended dynamic range of 95dB is presented. The accelerometer is fabricated in a low-resistivity (< 0.01Ω·cm) 120μm-thick silicon-on-insulator (SOI) substrate with extra seismic mass and small capacitive gaps using a high-yield dry-release fabrication process [2]. The capacitive sensitivity ($\Delta C/gravity$) is increased by reducing the gaps through post-deposition of doped low pressure chemical vapor deposited (LPCVD) polysilicon. The mechanical noise-floor per unit-area is improved by keeping a thick silicon seismic mass on the backside of the sensor. In contrast to previously reported ΔΣ micro-accelerometers, in which the mechanical transfer function of the sensor was typically the only element of the loop-filter [3], a switched-capacitor (SC) 2nd-order ΔΣ modulator is cascaded with the accelerometer and the front-end amplifier in this design. Having high capacitive sensitivity eliminates the requirement for high gain in the front-end and helps with better quantization noise shaping [4]. The accelerometer operates in air and is designed for a non-peaking response with a BW_{-3dB} of 500Hz.

The IC is implemented in a standard 3V 0.5μm N-well CMOS process. The output bitstream is amplified and fed back to the accelerometer through a set of comb-drive actuators. The main advantage of using comb drives (instead of a parallel-plate actuator) is that the electrostatic feedback force does not depend on the proof mass position, which improves linearity. Since the comb-drives are implemented in thick SOI with a reduced gap, the feedback force is strong enough to null the movement of the large proof mass. The measured output noise of the closed-loop system is -87dBV/√Hz at 20Hz. The system without electromechanical feedback has a measured noise floor of -65dBV/√Hz at 20Hz, which is dominated with the in-band quantization noise. A 22dB improvement in noise, and hence dynamic range, was achieved with a sampling clock of 40kHz, which corresponds to a low oversampling ratio (OSR) of 40. The interface IC draws 1.5mA from a 3V supply.

The fabrication process flow and the scanning electron microscope (SEM) picture of a device are shown in Fig. 16.1.1. The accelerometer is designed for a Brownian noise equivalent acceleration (BNEA) of 1μg/√Hz. The circuit noise equivalent acceleration (CNEA) is better than 1μg/√Hz. The measured total noise equivalent acceleration (TNEA) is 4μg/√Hz at 20Hz. Since the seismic mass is very large (10's of milli-gram) and the accelerometer is very compliant, the device is vulnerable to damage caused by mechanical shock. Therefore, deflection limiters are implemented to protect the accelerometer. Figure 16.1.2 shows the block diagram and *Z*-domain model of the system. The quantization-noise transfer function has a high-pass characteristic to up-convert the noise. Figure 16.1.3 shows the schematic of the IC interfaced with the accelerometer. This architecture relies on a front-end, including a programmable fully differential reference-capacitor-less SC charge amplifier, and a back-end, consisting of two cascaded SC integrators, a two-level quantizer and feedback networks. At the sensor-IC interface, the input switching is devised such that the charge amplifier can interface with four changing capacitances having *one common node* at the proof mass. The proof mass is biased with a DC voltage and is not switched, which helps reduce the switching noise. In previously reported fully-differential interfaces, there were typically two changing capacitors with a common node, requiring area-consuming on-chip reference capacitors to form a balanced capacitive bridge. In addition, the complexity of our design is reduced because there is not a distinct feedback clock phase. In other words, two comb drive actuators are dedicated to continuously apply the appropriate feedback force to the proof mass, and the output bitstream controls the average of the applied force. Correlated-double-sampling is used in the front-end to reduce flicker noise and offset. The core op amp in each block is a low-power low-noise fully differential folded-regulated cascode amplifier with a very high gain that improves the SC functionality and noise performance. The amplifier has a differential output swing of 4V from a 3V supply.

The accelerometer was wirebonded to the IC chip and the static and dynamic responses were tested. The measured accelerometer sensitivity is 5pF/g, an order-of-magnitude greater than the value reported in [1]. Figure 16.1.4 shows the open-loop and closed-loop responses of the system to DC and AC (50 milli-g peak at 0.6Hz) accelerations. CH1 shows the modulator's output bitstream and CH2 shows the charge amplifier's output (error signal). In the open-loop system, the error signal is large, meaning the proof mass displacement is large. In the closed-loop system, the output bitstream is applied to the comb-drive electrodes. The electrostatic feedback force pushes the seismic mass back to the null position and the error signal reduces significantly. Figure 16.1.5 shows the output noise spectrum of the accelerometer and IC combination, illustrating the noise shaping effect of the modulator and the up-conversion of the quantization noise. No in-band tones were observed in the output spectrum, which means the closed-loop system is functional for the input bandwidth of 500Hz. The closed-loop system provides 22dB of noise reduction, corresponding to a dynamic range of 95dB and a resolution of 15 bits at 20Hz. Figure 16.1.6 shows the summary of the measured specifications of the sensor and the interface IC. The die photo is shown in Figure 16.1.7. The area of the IC is 2.25mm^2.

References:

[1] B. V. Amini, et al., "A 2.5 V 14-Bit Sigma-Delta CMOS-SOI Capacitive Accelerometer," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2467–2476, Dec., 2004.

[2] B. V. Amini, et al., "Sub-Micro-Gravity Capacitive SOI Microaccelerometers," in *Proc. Transducers'05*, pp. 515-518.

[3] H. Kulah, et al., "A Multi-Step Electromechanical Sigma-Delta Converter for Micro-g Capacitive Accelerometers," in *ISSCC Dig. Tech. Papers*, pp. 202–203, Feb., 2003.

[4] V. P. Petkov, et al., "A Fourth-Order Sigma-Delta Interface for Micromachined Inertial Sensors," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1602–1609, Aug., 2005.

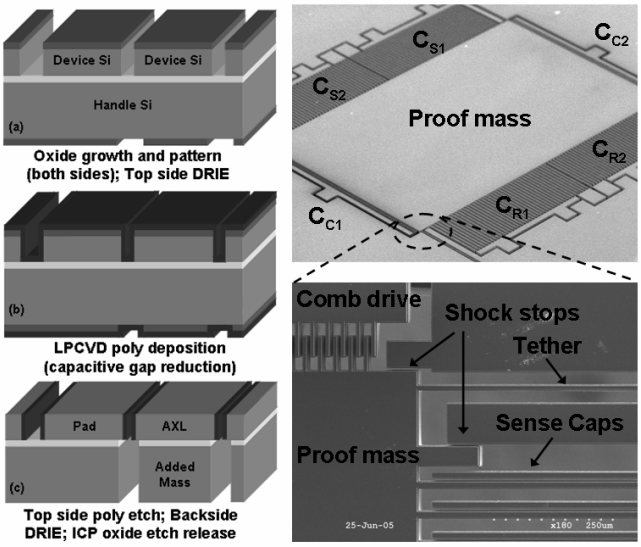

Figure 16.1.1: Accelerometer fabrication process; SEM views of the accelerometer.

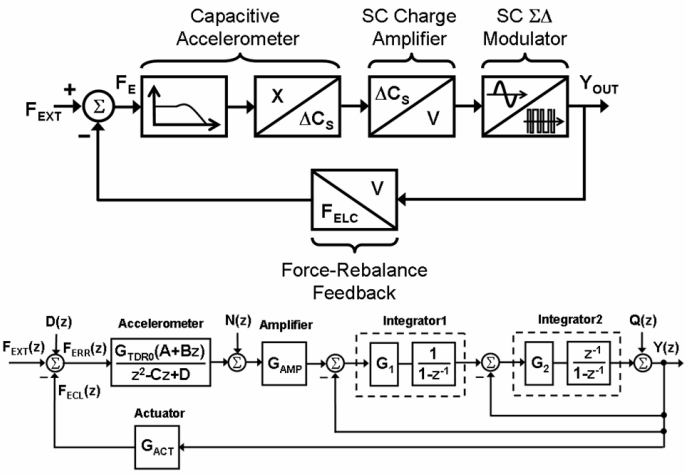

Figure 16.1.2: Closed-loop block diagram and Z-domain model.

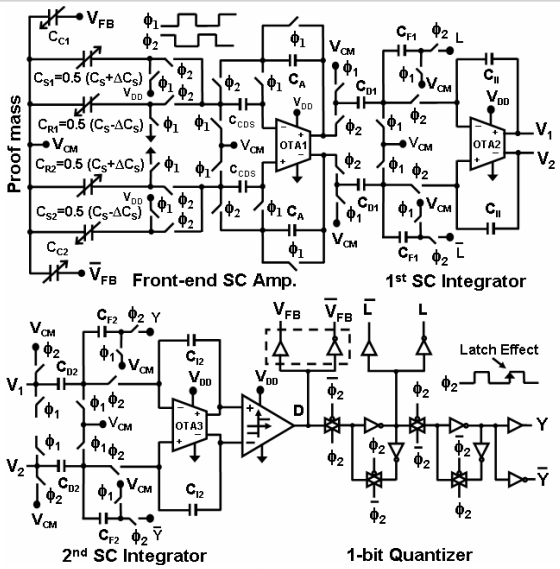

Figure 16.1.3: Circuit diagram of the ΔΣ accelerometer.

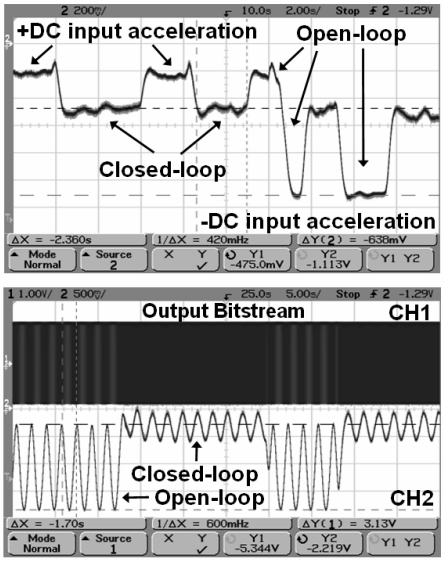

Figure 16.1.4: Measured time-domain response.

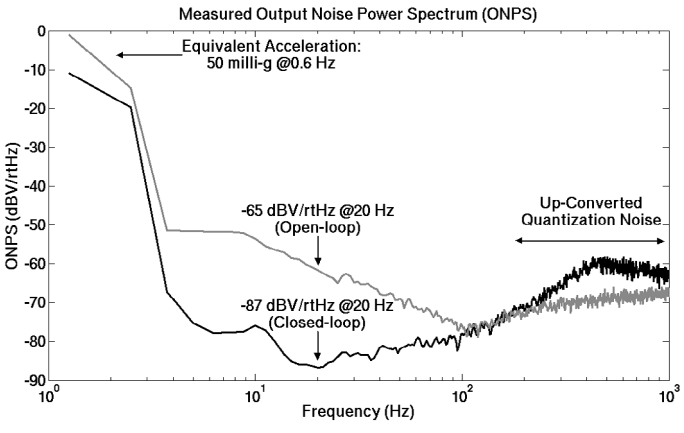

Figure 16.1.5: Measured output noise spectrum.

Closed-loop Microaccelerometer + IC Performance	
Proof mass size	3 mm × 5 mm
Overall sensor size	6 mm × 6 mm
Device thickness	120 µm
BNEA	1 micro-g/√Hz
Static sensitivity	5 pF/g
Sensor bandwidth	500 Hz
Front-end gain	30 V/g
Front-end Max. Diff. output swing	4 V (peak-to-peak & supply: 3 V-GND)
Bias stability	2 micro-g (for 12 hours)
Output noise	-87 dBV/ √Hz @ 20 Hz
TNEA	4 micro-g/√Hz @ 20 Hz
Capacitive resolution	2 aF/√Hz @ 20 Hz
Dynamic range	95 dB (15 bits of resolution)
Sampling clock	40 kHz
Power dissipation	4.5 mW (supply: 3 V-GND)
Chip area	2.25 mm^2

Figure 16.1.6: Measured specifications.

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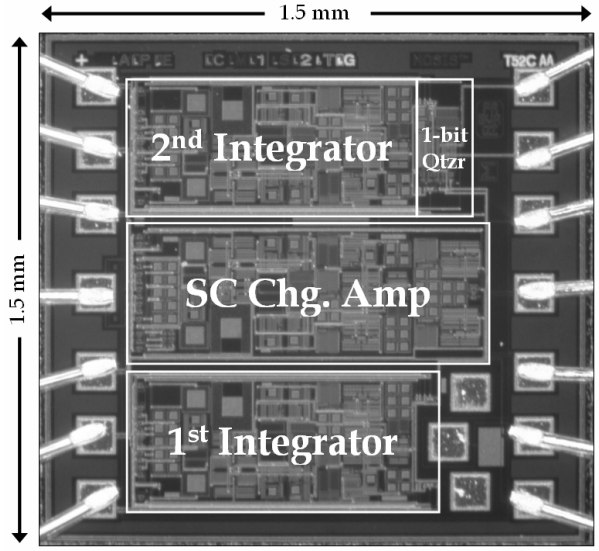

Figure 16.1.7: Die micrograph.

